WHAT IS CLAIMED IS:

1. A thin film transistor array panel comprising:

an insulating substrate;

an opaque film formed on the insulating substrate;

an insulating layer covering the opaque film and having a contact hole exposing the opaque film at least in part at a contact portion and having a plurality of boundaries, at least a portion of the boundaries located inside boundaries of the opaque film; and

a conductive layer formed on the insulating layer and connected to the opaque film through the contact hole,

wherein a distance between one of the boundaries of the contact hole of the contact portion at a place where alignment treatment or rubbing ends and one of the boundaries of the opaque film located outside the contact hole is wider than a distance between the boundaries of the contact holes at other places and the boundaries of the opaque film.

2. The thin film transistor array panel of claim 1, wherein the opaque film comprises a first wire and a second wire insulated from and overlapping the first wire and the second wire is exposed through the contact hole.

3. The thin film transistor array panel of claim 2, wherein one of boundaries of the first wire and the second wire is located outside the boundaries of the contact hole at the place where alignment treatment or rubbing ends.

4. The thin film transistor array panel of claim 3, wherein the first wire is either a gate wire or a storage capacitor wire, the second wire is either a data wire or a storage capacitor conductor, and the conductive layer is a pixel electrode made of transparent conductive material.

5. The thin film transistor array panel of claim 4, wherein the gate wire comprises a gate line and a gate electrode connected to the gate line, and the data wire comprises a data line intersecting the gate line, a source electrode connected to the data line and placed close to the gate electrode, and a drain electrode opposite the source electrode with respect to the gate electrode.

6. The thin film transistor array panel of claim 5, further comprising a gate insulating layer covering the gate wire, and a semiconductor layer formed on the gate insulating layer between the gate electrode and the source electrode and the drain electrode.

7. The thin film transistor array panel of claim 6, wherein the semiconductor layer has the same shape as the data wire except for a channel portion between the source electrode and the drain electrode.

8. The thin film transistor array panel of claim 4, wherein the storage capacitor wire comprises a storage capacitor line separated from the gate wire and a storage electrode connected to the storage capacitor line.

9. The thin film transistor array panel of claim 8, wherein the storage capacitor conductor is connected to the data wire.

10. The thin film transistor array panel of claim 1, wherein the insulating film comprises silicon nitride, organic insulating material or a low dielectric CVD film.